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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/722,306	11/28/2000	Yasunobu Iwata	Q61090	5612

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,306	IWATA ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-11* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 09/722,306 filed 11/28/2000 and amendment filed 09/08/2004.

2. Claims 1-11 remain pending in the Application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2 and 5-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Komiya et al. (US Patent 5,126,956).

With respect to claims 1 and 5 Komiya et al. teaches a ladder circuit editing system for inputting and editing a sequence program controller in the form of a ladder diagram within an apparatus and control system having a programmable sequence control function (abstract; col. 7, ll.58-61), comprising: an unavailable area for storing a plurality of previously stored circuit patterns of circuit elements within a buffer register (BFR) shown on the Fig. 11 as one of the elements of the Display controller (DPC) for storing the data such as the sequence program for storing the data of circuit element patterns (col. 8. 40-44; col. 9, ll.6-9), wherein a Display controller (DPC) shown on the Fig. 8 which is adapted to divide one line into an identification display area, a symbolic display area and an address display area to generate picture information to each display area (col. 7, ll.62-67); an available area for storing circuit elements of a circuit

pattern being input within a data register (RG) shown on the Fig. 11, wherein DPC is depicted in details and register (RG) is storing the data of the circuit elements such as the relay identification (CRA) (col. 8, ll.36-38) and wherein the register (RG) is coupled with input device (301g) for inputting the data of the desired circuit element (relay) to the register (RG) (available area) manually (col. 7, ll.49-50; col. 8, ll.22-30; col. 9, ll.6-11); circuit pattern extracting means for making a comparison between a circuit element stored in the available area and a corresponding circuit element contained in one of the plurality of previously stored circuit patterns in the unavailable area, and extracting from the plurality of previously stored circuit patterns an extracted circuit pattern in which the comparison indicates an agreement between the compared circuit elements within a comparator (COM) shown on the Fig. 11, which is coupled with register (RG) and buffer register (BFR) through discriminator (DIC) for performing the discrimination of the programmable code describing circuit elements for subjecting the data from register (RG) and buffer register (BFR) for the comparison and finding if there is agreement or nonagreement between the subjected data from register (RG) and buffer register (BFR) (col.9, ll.16-27); display means for displaying the extracted circuit pattern on an input screen within the cathode ray tube (CRT) as shown on the Fig. 8 (col. 7, ll.45-47), which coupled to the Display controller (DPC), where described above components are elements of the Universal Display Unit shown on the Fig. 8 for displaying the output of the processes having place in the Display Controller (DPC) for editing the data into picture information (, col. 7, ll.36-38; col. 8, ll.13-20); copying means for copying the extracted circuit pattern into the available area in response to an input by an operator

when comparison is finished and agreement between address and bit position for two items of data stored in register (RG) and buffer register (BFR) was reached, the data stored in BFR is converted into picture information, which is stored in the refresh memory (RFM) shown on the Fig. 11 (col. 9, ll.31-36).

With respect to claim 11 Komiya et al. teaches pre-storing a plurality of circuit patterns in a first storage area within a buffer register (BFR) shown on the Fig. 11 as one of the elements of the Display controller (DPC) for storing the data such as the sequence program for storing the data of circuit element patterns (col. 8. 40-44; col. 9, ll.6-9), wherein a Display controller (DPC) shown on the Fig. 8 which is adapted to divide one line into an identification display area, a symbolic display area and an address display area to generate picture information to each display area (col. 7, ll.62-67);inputting a new circuit pattern (col. 7, ll.48-50); storing the new circuit pattern in a second storage area within a data register (RG) shown on the Fig. 11, wherein DPC is depicted in details and register (RG) is storing the data of the circuit elements such as the relay identification (CRA) (col. 8, ll.36-38) and wherein the register (RG) is coupled with input device (301g) for inputting the data of the desired circuit element (relay) to the register (RG) (second area) manually (col. 7, ll.49-50; col. 8, ll.22-30; col. 9, ll.6-11); comparing the stored new circuit pattern with each of the pre-stored plurality of circuit patterns within a comparator (COM) shown on the Fig. 11, which is coupled with register (RG) and buffer register (BFR) through discriminator (DIC) for performing the discrimination of the programmable code describing circuit elements for subjecting the data from register (RG) and buffer register (BFR) for the comparison and finding if there

is agreement or nonagreement between the subjected data from register (RG) and buffer register (BFR) (col.9, ll.16-27); extracting each circuit pattern from the pre-stored plurality of circuit patterns that matches the stored new circuit pattern (col. 9, ll.26-30); displaying the each extracted circuit pattern on a screen (col. 8, ll.9-12); selecting each displayed pattern by an operator (col.17-20); copying the selected circuit pattern into the second storage area (col. 8, ll.36-38); wherein the comparison is performed by comparing each circuit element of the new circuit pattern with a corresponding circuit element from each circuit pattern of the stored plurality of circuit patterns within a comparator (COM) shown on the Fig. 11, which is coupled with register (RG) and buffer register (BFR) through discriminator (DIC) for performing the discrimination of the programmable code describing circuit elements for subjecting the data from register (RG) and buffer register (BFR) for the comparison and finding if there is agreement or nonagreement between the subjected data from register (RG) and buffer register (BFR) (col.9, ll.16-27).

With respect to claim 2 Komiya et al. teaches when more than one the extracted circuit pattern is extracted, the display means successively displays, for selection by an operator, the plurality of extracted circuit patterns within the ability of the Display controller (DPC) shown on the Fig. 11 to manipulate and selectively display by the operator (col. 8, ll.16-20); and in response to the selection of one of the plurality of extracted circuit patterns, the copying means copies the selected extracted circuit pattern into the available area as shown on the Fig. 12 the ladder segment was selected for being input into DPC and stored in the register (RG) (col. 9, ll.2-4).

With respect to claims 6-9 Komiya et al. teaches

Claim 6: selecting means for receiving another input from the operator, wherein another input if whether the extracted circuit pattern is to be stored within the comparator (COM) shown on the Fig. 11, wherein if the nonagreement between the subjected data from register (RG) and buffer register (BFR) was found then a request for next input from operator is generated (col. 8, ll.56-59);

Claim 7: when the inputted circuit element of the inputted pattern is in activation division, the extracting means compares the inputted circuit element with the stored circuit elements of an activation division of one stored circuit pattern of the plurality if circuit patterns by using the preparation of the comparison within controller (CNT) shown on the Fig. 11 by comparator (COM) for subjecting the data from register (RG) and buffer register (BFR) for the comparison and finding if there is agreement or nonagreement between the subjected data from register (RG) and buffer register (BFR) (col. 8, ll.37-41; col.9, ll.16-27);

Claim 8: when the circuit element from the inputted circuit elements, is in an interlock division of the inputted circuit pattern, the extracting means compares the circuit elements with the corresponding circuit elements being in an interlock division of one of the plurality of previously stored circuit pattern (col. 8, ll.56-61);

Claim 9; when the circuit element from the inputted circuit elements, is in an output division of the inputted circuit pattern, the extracting means compares the circuit element with the corresponding circuit elements being in an output division of one of the plurality of previously stored circuit patterns within controller (CNT) (col. 9, ll.25-30);

Claim 10: when the extracting means extracts more than one circuit patterns, the selecting means sequentially asks the operator for the another input for each of the more than one circuit patterns (col. 9, ll.28-30);

Allowable Subject Matter

Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach wherein the display means displays a previously selected circuit pattern as a top priority, wherein the display means displays as a top priority the previously selected circuit pattern according to an order of address stored in the selected circuit pattern address storage area.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
Technology Center 2800